REMARKS

Claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 are pending in the application.

35 USC 112 Second Paragraph Rejection of Claims 11 and 12

The Office Action rejected claims 11 and 12 as allegedly being indefinite under 35 USC 112.

Claims 11 and 12 have been reviewed and are amended where appropriate. It is respectfully submitted that claims 11 and 12 are now in full conformance with 35 USC 112. It is respectfully requested that the rejection be withdrawn.

Claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 over Tal and Old and Well-Known Prior Art

In the Office Action, claims 1-3, 6, 8, 10-12, 15, 17, 19-21, 24 and 26 were rejected under 35 U.S.C. §102(e) as allegedly being anticipated by U.S. Patent No. 6,662,254 to Tal et al. ("Tal"), with claims 5, 7, 14, 16, 23 and 25 rejected under 35 U.S.C. §103(a) as allegedly being obvious over Tal in view of old and well-known prior art. The Applicants respectfully traverse the rejection.

The Office Action cites a Tai et al. ("Tai") reference for rejecting 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 without proving a Tai reference on a PTO-892. A telephone call to the Examiner verified the intended reference for rejecting claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 is Tal. The Applicants are herein responding to Tal.

Claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 a method and apparatus relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application.

Tal appears to discloses a serial channel consisting of a pair of PCI serializer/deserializers that are used to connect PCI bus segments (col. 6, lines 11-17; Fig. 8). The serial channel is built out of 4 full duplex pairs, each providing 622 mbps of bandwidth (Tal, col. 6, lines 18-22).

Tal discloses use of 4 full duplex pairs. However, in situations where less bandwidth is needed to connect two PCI bus segments, Tal still relies on 4 full duplex pairs. Tal fails to disclose or suggest a method and apparatus relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application, as recited by claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26.

Claims 5, 14 and 23 recite a method and apparatus relying on a first half bridge circuit and a second half bridge circuit connecting a first bus segment bus frequency that is different than a second bus segment bus frequency.

The Examiner alleges that the use of the use of two PCI buses having different frequencies is old and well-known as evidenced by Lange (See Office Action, page 5). The Applicants respectfully disagree.

The Applicants' claims are not simply claiming two PCI buses having different frequencies as alleged by the Examiner. The Applicants' claimed features recite connecting two PCI bus segments having different frequencies, more specifically with a first half bridge circuit and a second half bridge circuit, as recited by claims 5, 14 and 23.

A review of Lange fails to disclose or suggest connecting PCI busses having different frequencies, much less with half bridge circuits, i.e., a method and apparatus relying on a first half bridge circuit and a second half bridge circuit connecting a first bus segment bus frequency that is different than a second bus segment bus frequency, as recited by claims 5, 14 and 23.

Claims 7, 16 and 25 recite a method and apparatus relying on at least one of a first half bridge circuit and a second half bridge circuit are field programmable.

The Examiner takes Official Notice that the use of FPSC for a PCI half bridge is old and well-known as evidenced by the acknowledged prior art (See Office Action, page 5). The Applicants respectfully disagree.

The Applicants' "Background of Related Art" discloses FPSC for use with conventional PCI solutions. However, the "Background of Related Art" fails to disclose or suggest application of programmability to Applicants' claimed half bridge circuit. Thus, the Examiner is requested to **support** the allegation that it is old and well-known within the art to apply field programmability principles to a half bridge circuit, i.e., a method and apparatus relying on at least one of a first half bridge circuit and a second half bridge circuit are field programmable, as recited by claims 7, 16 and 25.

A benefit of a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application is, e.g., reduced power consumption. When bandwidth requirements between two bus segments is low, less than the maximum number of circuitry supporting data paths between two bus segments is needed. Thus, a scalable architecture a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit reduces aggregate power consumption while still fulfilling data transfer needs. The cited prior art fails to disclose or **suggest** the claimed features having such benefits.

Accordingly, for at least all the above reasons, claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 over Nakamura and Old and Well-Known Prior Art

In the Office Action, claims 1-3, 6, 8, 10-12, 15, 17, 19-21, 24 and 26 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over U.S. Patent No. 6,606,678 to Nakamura ("Nakamura"), with claims 5, 7, 14, 16, 23 and 25 rejected under 35 U.S.C. §103(a) as allegedly being obvious over Nakamura in view of old and well-known prior art. The Applicants respectfully traverse the rejection.

Claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 recite a method and apparatus relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application.

Nakamura discloses a PCI-PCI bridge for connecting a primary PCI bus to a secondary PCI bus (Abstract). The PCI-PCI bridge allows the connection of a notebook type personal computer to a docking station through a cable (Nakamura, col. 5, lines 1-10). A single serial data path is used to connect the primary PCI bus to the second PCI bus (Nakamura, Fig. 1, item 300).

Although Nakamura discloses a PCI-PCI bridge, only a single serial data path is used to connect a primary PCI bus to a second PCI bus. Thus, Nakamura fails to disclose or **suggest** a method and apparatus relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application, as recited by claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26.

Claims 5, 14 and 23 recite a method and apparatus relying on a first half bridge circuit and a second half bridge circuit connecting a first bus segment bus frequency that is different than a second bus segment bus frequency.

The Examiner alleges that the use of the use of two PCI buses having different frequencies is old and well-known as evidenced by Lange (See Office Action, page 7). The Applicants respectfully disagree.

As discussed above, The Applicants' claims are not simply claiming two PCI buses having different frequencies as alleged by the Examiner. The Applicants' claimed features recite connecting two PCI bus segments having different frequencies, more specifically with a first half bridge circuit and a second half bridge circuit, as recited by claims 5, 14 and 23.

A review of Lange fails to disclose or suggest connecting PCI busses having different frequencies, much less with half bridge circuits, i.e., a method and apparatus relying on a first half bridge circuit and a second half bridge circuit connecting a first bus segment bus frequency that is different than a second bus segment bus frequency, as recited by claims 5, 14 and 23.

Claims 7, 16 and 25 recite a method and apparatus relying on at least one of a first half bridge circuit and a second half bridge circuit are field programmable.

The Examiner takes Official Notice that the use of FPSC for a PCI half bridge is old and well-known as evidenced by the acknowledged prior art (See Office Action, page 8). The Applicants respectfully disagree.

As discussed above, the Applicants' "Background of Related Art" discloses FPSC for use with conventional PCI solutions. However, the "Background of Related Art" fails to disclose or suggest application of programmability to Applicants' claimed half bridge circuit. Thus, the Examiner is requested to **support** the allegation that it is old and well-known within the art to apply programmability principles to a half bridge circuit, i.e., a method and apparatus relying on at least one of a first half bridge circuit and a second half bridge circuit are field programmable, as recited by claims 7, 16 and 25.

Accordingly, for at least all the above reasons, claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 1-3, 6, 7, 10-12, 14-16, 19-21 and 23-25 over Lange and Old and Well-Known Prior Art

In the Office Action, claims 1-3, 10-12, 14, 19-21 and 23 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over U.S. Patent No. 6,457,091 to Lange et al. ("Lange"), with claims 6, 7k, 15, 16, 24 and 25 rejected under 35 U.S.C. §103(a) as allegedly being obvious Lange in view of old and well-known prior art. The Applicants respectfully traverse the rejection.

Claims 1-3, 6, 7, 10-12, 14-16, 19-21 and 23-25 recite a method and apparatus relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application.

Lange appears to rely on a high speed connector 112 to connect a first half bridge PCI circuit and a second half bridge PCI circuit (Fig. 4). The high speed connection is disclosed as being a serial gigabit Ethernet link (Lange, col. 4, lines 1-12).

Lange discloses a first half bridge PCI circuit connected to a second half bridge PCI circuit over an Ethernet link. Thus, Lange fails to disclose or suggest any type of scalability to the connection of the first half bridge PCI circuit connected to a second half bridge PCI circuit, i.e. fails to disclose or suggest a method and apparatus relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application, as recited by claims 1-3, 6, 7, 10-12, 14-16, 19-21 and 23-25.

Claims 7, 16 and 25 recite a method and apparatus relying on at least one of a first half bridge circuit and a second half bridge circuit are field programmable.

The Examiner takes Official Notice that the use of FPSC for a PCI half bridge is old and well-known as evidenced by the acknowledged prior art (See Office Action, page 10). The Applicants respectfully disagree.

As discussed above, the Applicants' "Background of Related Art" discloses FPSC for use with conventional PCI solutions. However, the

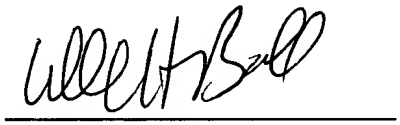
"Background of Related Art" fails to disclose or suggest application of programmability to Applicants' claimed half bridge circuit. Thus, the Examiner is requested to **support** the allegation that it is old and well-known within the art to apply field programmability principles to a half bridge circuit, i.e., a method and apparatus relying on at least one of a first half bridge circuit and a second half bridge circuit are field programmable, as recited by claims 7, 16 and 25.

Accordingly, for at least all the above reasons, claims 1-3, 6, 7, 10-12, 14-16, 19-21 and 23-25 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,



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